RTL8711AF

SINGLE-CHIP 802.11b/g/n 1T1R WLAN SoC

Pre-Release DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.0	2014/09/30	Preliminary release.
0.0	2015/03/05	update PINMUX table
R1V4	2015/09/25	1. correct feature list 2. modify block diagram 3. correct programming space, IO space and extension memory space 4. correct pin function group table 5. correct memory system 6. modify electrical characteristics
R1V5	2015/10/30	1. correct features of UART
R1v6	2016/1/7	1. correct source clock of timer
R1V7	2016/2/16	1. correct pin function group table
R1V8	2016/5/13	1. correct power on trap table
R1V9	2016/10/25	1. modify boot scenario description 2. Modify pin mux table 3. add io characteristic table 4. add LS-UART 5. add power sequence
R1V10	2017/2/8	1. correct package specification

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1. General Description

Realtek RTL8711AF is a highly integrated single-chip low power 802.11n Wireless LAN (WLAN) network controller. It combines an ARM-CM3 MCU, WLAN MAC, a 1T1R capable WLAN baseband, and RF in a single chip. It also provides a bunch of configurable GPIOs which are configured as digital peripherals for different applications and control usage.

RTL8711AF integrates internal memories for complete WIFI protocol functions. The embedded memory configuration also provides simple application developments.

2. Features

General

- Package QFN48 (6x6mm^2)
- CMOS MAC, Baseband PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
- Complete 802.11n solution for 2.4GHz band
- 72.2Mbps receive PHY rate and 72.2Mbps transmit PHY rate using 20MHz bandwidth
- 150Mbps receive PHY rate and 150Mbps transmit PHY rate using 40MHz bandwidth
- Compatible with 802.11n specification
- Backward compatible with 802.11b/g devices while operating in 802.11n mode

Standards Supported

- 802.11b/g/n compatible WLAN
- 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- WIFI WPS support
- WIFI Direct support
- Light Weight TCP/IP protocol

WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- Power saving mechanism

WLAN PHY Features

- 802.11n OFDM
- One Transmit and one Receive path (1T1R)
- 20MHz and 40MHz bandwidth transmission
- Short Guard Interval (400ns)

- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, and 640QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC

Peripheral Interfaces

- SDIO Slave
- Maximum 2 high speed UART interface with baud rate up to 4MHz
- 1 log UART with standard baud rate support
- Maximum 3 I^2C interface
- I^2S with 8/16/24/32/48/96/44.1/88.2 KHz sampling rate
- Maximum 2 PCM with 8/16KHz sample rate
- Maximum 2 SPI supported with baud rate up to 41.5MHz.
- Support 4 PWM with configurable duration and duty cycle from 0 ~ 100%
- Support 4 External Timer Trigger Event (ETE function) with configurable period in low power mode
- Maximum 21 GPIO pins

3. Block Diagram

3.1. Functional Block Diagram

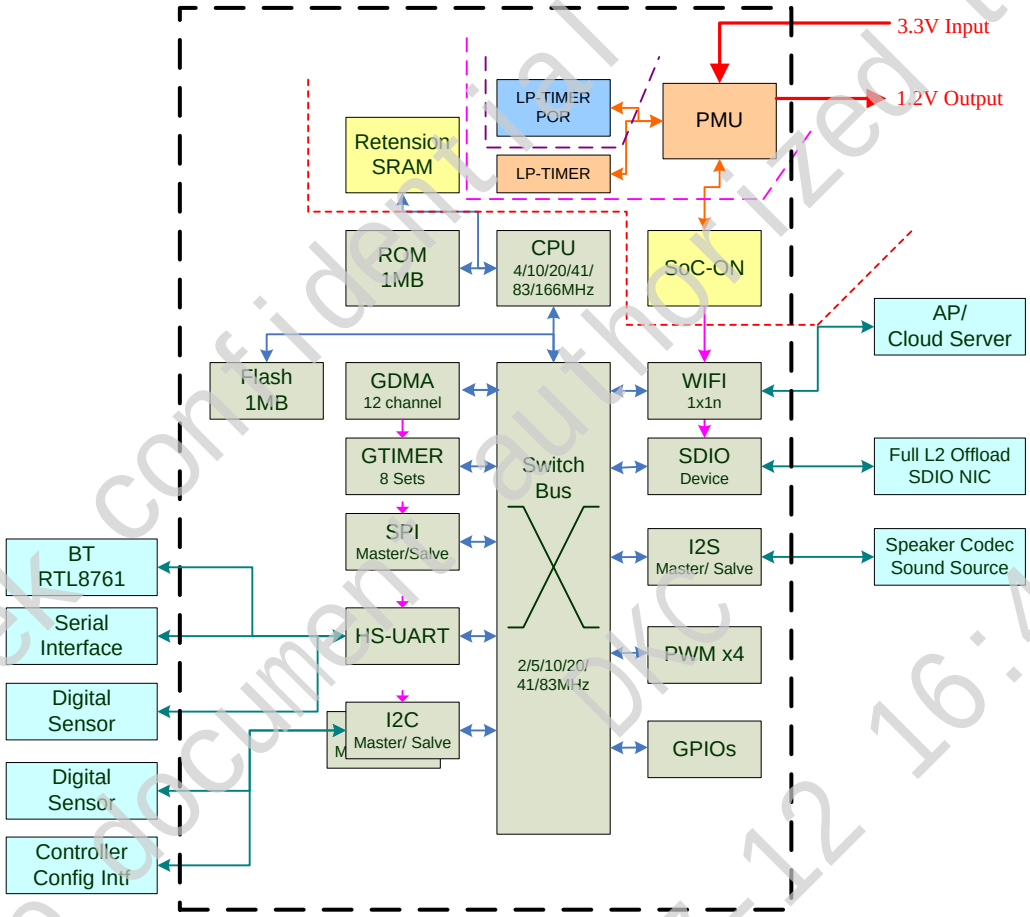


Figure 1. Block Diagram

3.2. WIFI and NFC Application Diagram

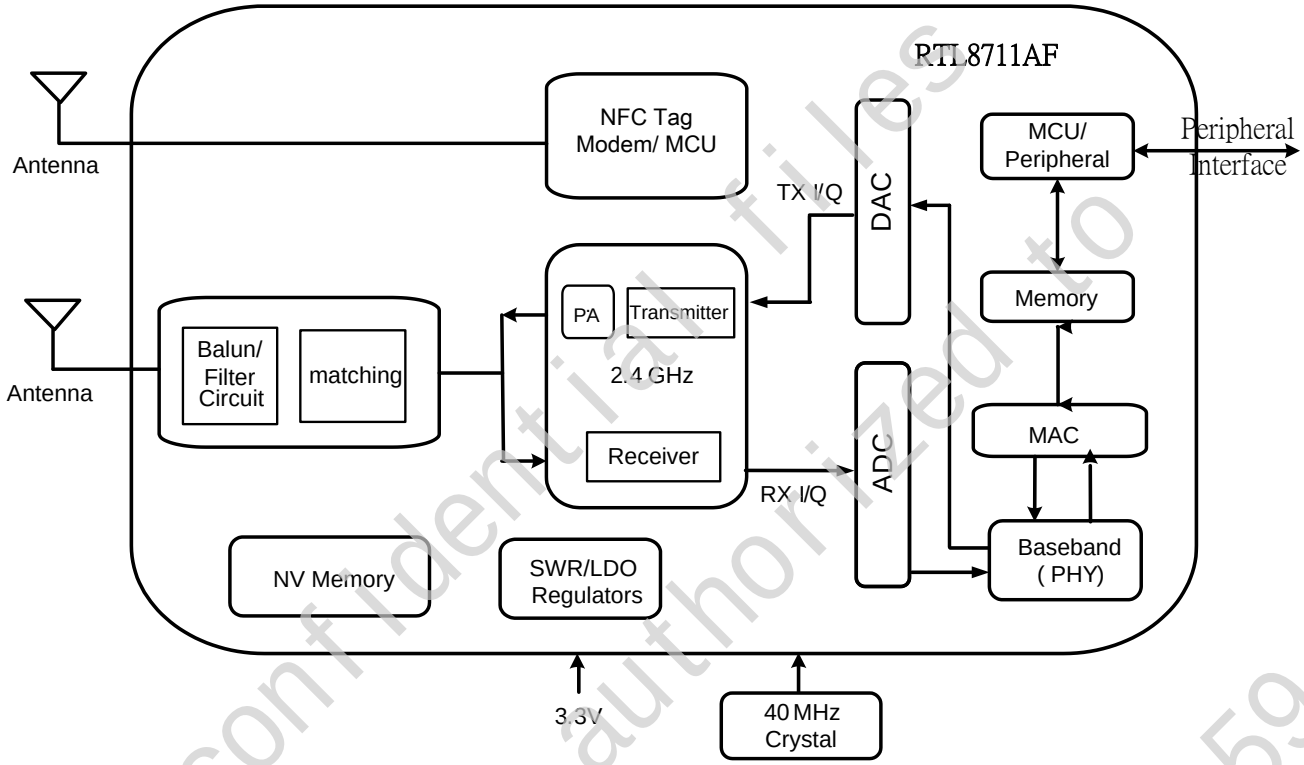


Figure 2. Single-Band 11n (1x1) and NFC Tag Solution

3.3. Power Supply Application Diagram

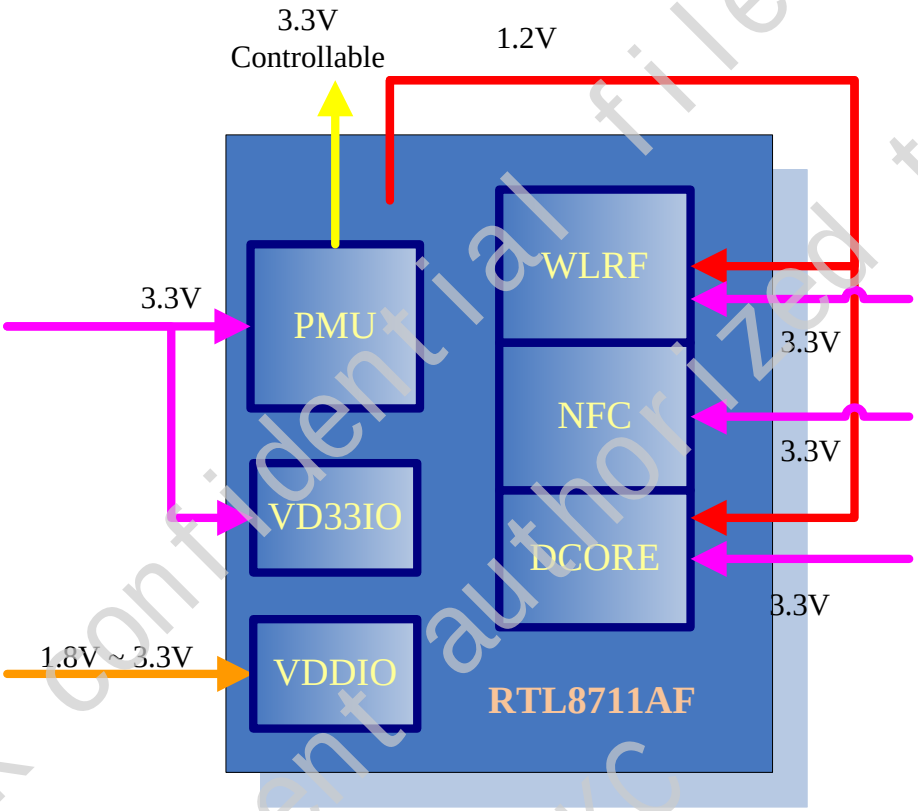


Figure 3. Power Supply Architecture

The integrated Power Management Unit (PMU) provides the following features:

- 1.2V power bulk or LDO selectable.
- 3.3V power source integrated power cut controlled by FW.

4. Memory Mapping

4.1. Programming Space

Name	Mode	Physical	Size	IP Function
Code		0x0000_0000 0x000F_FFFF	1MB	Instruction Memory (ROM)
		0x1000_0000 0x1006_FFFF	448KB	Inter SRAM: BD SRAM and Buffer SRAM share total 448KB physical sram
		0x1FFF_0000 0x1FFF_FFFF	64KB	TCM (Tightly-Coupled Memory) SRAM

4.2. IO Space

Name	Mode	Physical	Size	IP Function
Peripheral		0x4000_0000	4KB	SYS Control (SYSON)
		0x4000_0FFF		
		0x4000_1000	2KB	GPIO Control
		0x4000_17FF		
		0x4000_1800		RSVD
		0x4000_1FFF		
		0x4000_2000	4KB	Timer Control
		0x4000_2FFF		
		0x4000_3000	1KB	UART for Log
		0x4000_33FF		
		0x4000_3400	1KB	I2C_2 Control
		0x4000_37FF		
		0x4000_3800	1KB	I2C_3 Control
		0x4000_3BFF		
		0x4000_3C00		RSVD
		0x4000_4FFF		
		0x4000_5000	4KB	SDR SDRAM controller
		0x4000_5FFF		
		0x4000_6000	4KB	SPI flash controller
		0x4000_6FFF		
		0x4000_7000		RSVD
		0x4000_FFFF		
		0x4001_0000	4KB	ADC
		0x4001_0FFF		
		0x4001_1000	4KB	DAC
		0x4001_1FFF		

Name	Mode	Physical	Size	IP Function
Peripheral		0x4004_0000	1KB	UART_0 Control
		0x4004_03FF		
		0x4004_0400	1KB	RSVD
		0x4004_07FF		
		0x4004_0800	1KB	UART_2 Control
		0x4004_0BFF		
		0x4004_0C00		RSVD
		0x4004_1FFF		
		0x4004_2000	1KB	SPI_0 Control
		0x4004_23FF		
		0x4004_2400	1KB	SPI_1 Control
		0x4004_27FF		
		0x4004_2800	1KB	RSVD
		0x4004_2BFF		
		0x4004_2C00		RSVD
		0x4004_3FFF		
		0x4004_4000	1KB	RSVD
		0x4004_43FF		
		0x4004_4400	1KB	I2C_1 Control
		0x4004_47FF		
		0x4004_4800		RSVD
		0x4004_FFFF		

Name	Mode	Physical	Size	IP Function
Peripheral		0x4005_0000	16KB	RSVD
		0x4005_3FFF		
		0x4005_4000		RSVD
		0x4005_7FFF		
		0x4005_8000	16KB	SDIO Host
		0x4005_BFFF		
		0x4005_C000		RSVD
		0x4005_FFFF		
		0x4006_0000	2KB	GDMA0
		0x4006_07FF		
		0x4006_0800	2KB	RSVD for other DMA
		0x4006_0FFF		
		0x4006_1000	2KB	GDMA1
		0x4006_17FF		
		0x4006_1800		RSVD for other DMA
		0x4006_1FFF		

Name	Mode	Physical	Size	IP Function
Peripheral		0x4006_2000 0x4006_23FF	1KB	RSVD
		0x4006_2400 0x4006_2FFF	3KB	RSVD
		0x4006_3000 0x4006_33FF	1KB	I2S_1 Control
		0x4006_3400 0x4006_3FFF	3KB	RSVD
		0x4006_4000 0x4006_43FF	1KB	PCM_0 Control
		0x4006_4400 0x4006_4FFF		RSVD
		0x4006_5000 0x4006_53FF	1KB	PCM_1 Control
		0x4007_0000 0x4007_3FFF	16KB	Security Engine
		0x4007_4000 0x4007_FFFF	48KB	RSVD
		0x4008_0000 0x400B_FFFF	256KB	WIFI REG & TX/RX FIFO direct map
		0x400C_0000 0x400F_FFFF	256KB	RSVD
		0x403F_FFFF	1MB	RSVD

4.3. Extension Memory Space

Name	Mode	Physical	*Size*	IP Function
Flash		0x9800_0000 0x9810_0000	1MB	External flash memory

5. Pin Assignments

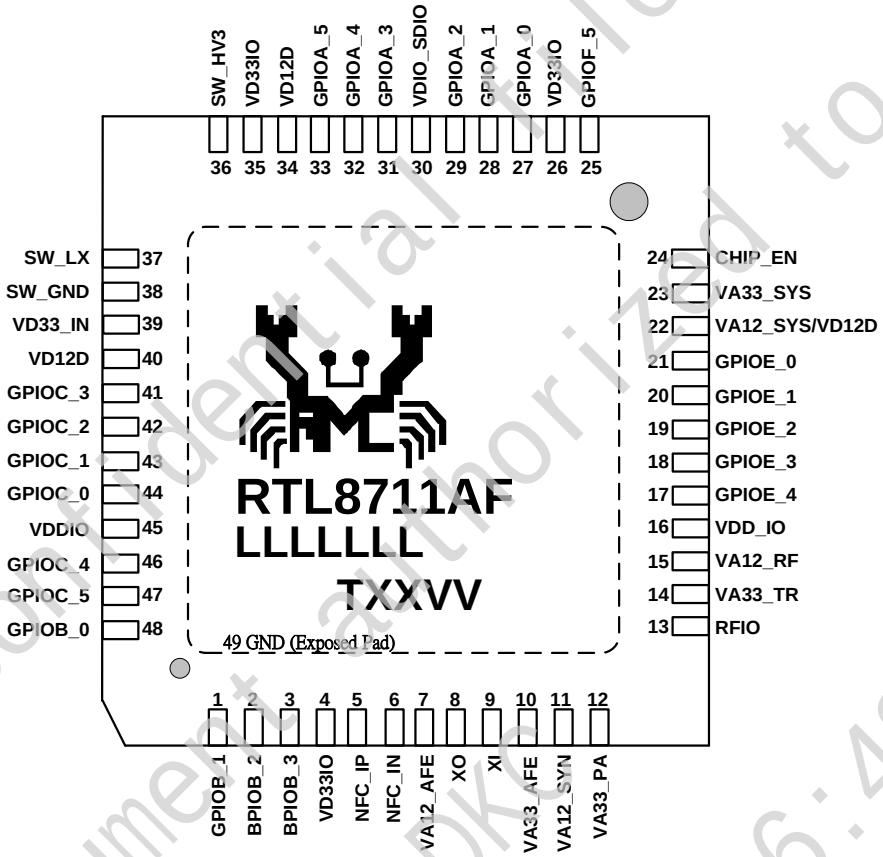


Figure 4. Pin Assignments

5.1. Package Identification

The version is shown in the location marked 'VV' in Figure 4, e.g., A0=Version A0

6. Pin Descriptions

The following signal type codes are used in the tables:

I:	Input	O:	Output
T/S:	Tri-State bi-directional input/output pin	S/T/S:	Sustained Tri-State
O/D:	Open Drain	P:	Power pin

6.1. Power On Trap Pin

Table 1. Power On Trap Pins

Symbol	Type	Pin No	Description
NORMAL_MODE_SEL	I	2	Shared with GPIOB_2 1: Normal operation mode 0: Enter into test/debug mode
BOOT_SCENARIO	I	48	Shared with GPIOB_0 0: Normal booting 1: Reserved for RTK testing
EEPROM_SEL	I	25	Shared with GPIOF_5 0: Internal NV memory select 1: Reserved for RTK testing
ICFG0	I	44	Shared with GPIOC_0 When NORMAL_MODE_SEL is “0”, then ICFG0 is test mode BIT0.
ICFG1	I	43	Shared with GPIOC_1 When NORMAL_MODE_SEL is “0”, then ICFG1 is test mode BIT1.
ICFG2	I	42	Shared with GPIOC_2 When NORMAL_MODE_SEL is “0”, then ICFG2 is test mode BIT2.

Symbol	Type	Pin No	Description
ICFG3	I	41	Shared with GPIOC_3 When NORMAL_MODE_SEL is “0”, then ICFG3 is test mode BIT3.

6.2. RF and NFC

Table 2. RF and NFC Pins

Symbol	Type	Pin No	Description
NFC_IP	I	5	NFC input differential signal
NFC_IN	I	6	NFC input differential signal
RF_IO	IO	13	WL RF signal

NOTE: The unused pins are suggested to keep floating.

6.3. Power Pins

Table 3. Power Pins

Symbol	Type	Pin No	Description
SW_LX	P	37	Switching Regulator Output
SW_HV3	P	36	Switching Regulator Input Or Linear Regulator input from 3.3V to 1.2V
VA33	P	10, 12, 14, 23	3.3V for Analog Circuit
VD33IO	P	4, 26, 35, 39	VDD3.3V for Digital IO or digital blocks
VDD_IO	P	16, 45	GPIOE and GPIOC group IO power
VDIO_SDIO	P	30	SDIO Bus IO power
VD12D	P	34, 40	VDD 1.2V Digital Circuit
VA12	P	7, 11, 15, 22	1.2V for analog blocks
SW_GND	P	38	Switching Regulator Ground

6.4. Clock Pins

Table 4. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	9	40MHz OSC Input Input of 40MHz Crystal Clock Reference
XO	O	8	Output of 40MHz Crystal Clock Reference

6.5. Chip Enable Pin

Table 5. Chip Enable Pin

Symbol	Type	Pin No	Description
CHIP_EN	I	29	Whole chip enable control. When asserted, chip function is enabled; when de-asserted, whole chip is shutdown.

6.6. Digital IO Pins

Please refer to section 6 Pin Function Table for more detailed information.

Table 6. IO Pins

Symbol	Type	Pin No	Description
GPIOB_0	IO	48	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOB_1	IO	1	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOB_2	IO	2	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOB_3	IO	3	GPIO pin. The MUX function can be referred to Pin Function Table.

Symbol	Type	Pin No	Description
GPIOE_0	IO	21	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOE_1	IO	20	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOE_2	IO	19	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOE_3	IO	18	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOE_4	IO	17	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOA_0	IO	27	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOA_1	IO	28	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOA_2	IO	29	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOA_3	IO	31	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOA_4	IO	32	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOA_5	IO	33	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOC_0	IO	44	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOC_1	IO	43	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOC_2	IO	42	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOC_3	IO	41	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOB_4	IO	46	GPIO pin. The MUX function can be referred to Pin Function Table.
GPIOB_5	IO	47	GPIO pin. The MUX function can be referred to Pin Function Table.

NOTE: GPIO group F is not open for customer.

NOTE: The unused pins are suggested to keep floating.

Table 7. GPIO Characteristic

Symbol	Interrupt	Schmitt trigger	Driving[1] (mA)	Default state[2]	Sleep Mode, shutdown
GPIOB_0	N	N	8/16 (Configurable)	HI	Input/Output; PU, PD or HI (Configurable)
GPIOB_1	N	N	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOB_2	N	Y	8/16 (Configurable)	HI	Input/Output; PU, PD or HI (Configurable)
GPIOB_3	Y	N	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOE_0	N	Y	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOE_1	Y	Y	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOE_2	Y	Y	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOE_3	Y	Y	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOE_4	N	Y	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOA_0	Y	Y	3.8/7.6/11/15/19/23/26 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOA_1	Y	N	3.8/7.6/11/15/19/23/26 (Configurable)	PH	Input/Output; PD or HI (Configurable)
GPIOA_2	N	Y	3.8/7.6/11/15/19/23/26 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOA_3	N	Y	3.8/7.6/11/15/19/23/26 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)

Symbol	Interrupt	Schmitt trigger	Driving[1] (mA)	Default state[2]	Sleep Mode, shutdown
GPIOA_4	N	N	3.8/7.6/11/15/19/23/26 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOA_5	N	N	3.8/7.6/11/15/19/23/26 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOC_0	N	N	8/16 (Configurable)	HI	Input/Output; PU, PD or HI (Configurable)
GPIOC_1	Y	Y	8/16 (Configurable)	HI	Input/Output; PU, PD or HI (Configurable)
GPIOC_2	N	N	8/16 (Configurable)	HI	Input/Output; PU, PD or HI (Configurable)
GPIOC_3	Y	Y	8/16 (Configurable)	HI	Input/Output; PU, PD or HI (Configurable)
GPIOC_4	Y	N	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)
GPIOC_5	Y	Y	8/16 (Configurable)	PH	Input/Output; PU, PD or HI (Configurable)

NOTE1: The driving configuration is operated by group.
NOTE2: PH = Pull-High, HI = High-impedance
NOTE3 : GPIOA_1 needs external Circuit to do the pull high control; others' pull control can be done by register setting (including GPIOA_1's PD)

6.7. SDIO Interface

Table 8. SDIO Transceiver Interface

Symbol	Type	Pin No	Description
GPIOA_0	IO	27	SDIO bus SD_D2
GPIOA_1	IO	28	SDIO bus SD_D3
GPIOA_2	IO	29	SDIO bus SD_CMD
GPIOA_3	IO	31	SDIO bus SD_CLK
GPIOA_4	IO	32	SDIO bus SD_D0
GPIOA_5	IO	33	SDIO bus SD_D1

NOTE: The unused pins are suggested to keep floating.

7. Pin Function Table

7.1. Pin Configurable Function Group Summary Table

Table 9. Pin Function Group Table

PIN name	JTAG	SDIO	UART Group	I2C Group	SPI Group	I2S Group	PCM Group	WL_LED	PWM	ETE	WKDT
GPIOA_0		SD_D2	UART2_IN		SPI1_MISO						
GPIOA_1		SD_D3	UART2_CTS		SPI1_MOSI						
GPIOA_2		SD_CMD	UART2_RTS		SPI1_CLK						
GPIOA_3		SD_CLK									
GPIOA_4		SD_D0	UART2_OUT		SPI1_CS						
GPIOA_5		SD_D1									D_SBY0
GPIOB_0			UART_LOG_OUT							ETE0	
GPIOB_1			UART_LOG_IN					WL_LED0		ETE1	D_SLP0
GPIOB_2				I2C3_SCL						ETE2	
GPIOB_3				I2C3_SDA						ETE3	
GPIOC_0			UART0_IN		SPI0_CS0	I2S1_WS	PCM1_SYNC		PWM0	ETE0	
GPIOC_1			UART0_CTS		SPI0_CLK	I2S1_CLK	PCM1_CLK		PWM1	ETE1	
GPIOC_2			UART0_RTS		SPI0_MOSI	I2S1_SD_TX	PCM1_OUT		PWM2	ETE2	
GPIOC_3			UART0_OUT		SPI0_MISO	I2S1_MCK	PCM1_IN		PWM3	ETE3	
GPIOC_4				I2C1_SDA	SPI0_CS1	I2S1_SD_RX					
GPIOC_5				I2C1_SCL	SPI0_CS2						
GPIOE_0	JTAG_TRST		UART0_OUT	I2C2_SCL	SPI0_CS0		PCM0_SYNC		PWM0		
GPIOE_1	JTAG_TDI		UART0_RTS	I2C2_SDA	SPI0_CLK		PCM0_CLK		PWM1		
GPIOE_2	JTAG_TDO		UART0_CTS	I2C3_SCL	SPI0_MOSI		PCM0_OUT		PWM2		
GPIOE_3	JTAG_TMS		UART0_IN	I2C3_SDA	SPI0_MISO		PCM0_IN		PWM3		D_SBY3
GPIOE_4	JTAG_CLK				SPI0_CS1						

NOTE1: The Function Pin is enabled via entire group, the un-used pin can not disable separately. Ex: if using JTAG in SWD mode, the pin: JTAG_TRST, JTAG_TDI and JTAG_TDO can not be used as GPIO in the same time.

NOTE2: GPIO group F is not open for customer.

8. Functional Description

8.1. Power Management Control Unit

8.1.1. Features

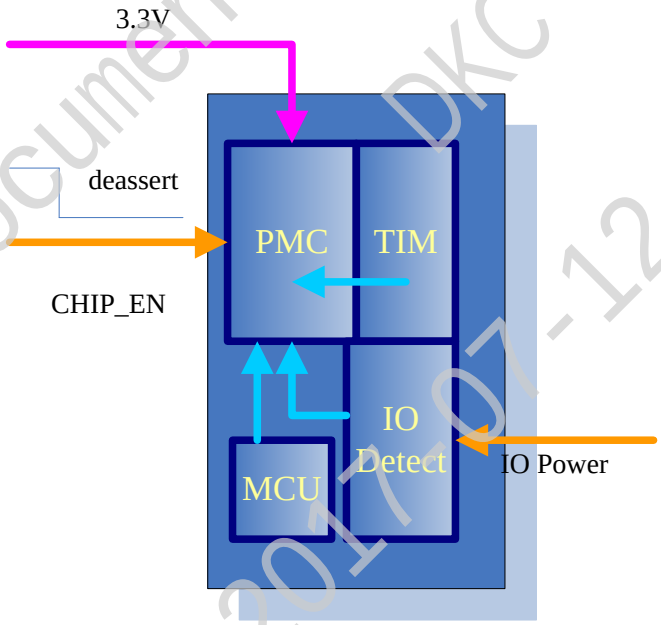
The PMU provides the following functions:

- Bulk/LDO to output 1.2V
- 2 very Low power clock source with less accuracy: 1K and 500K
- 1 low power 32.768KHz clock source with moderate accuracy
- Wakeup system detector to resume from low power state

8.1.2. Power Mode Description

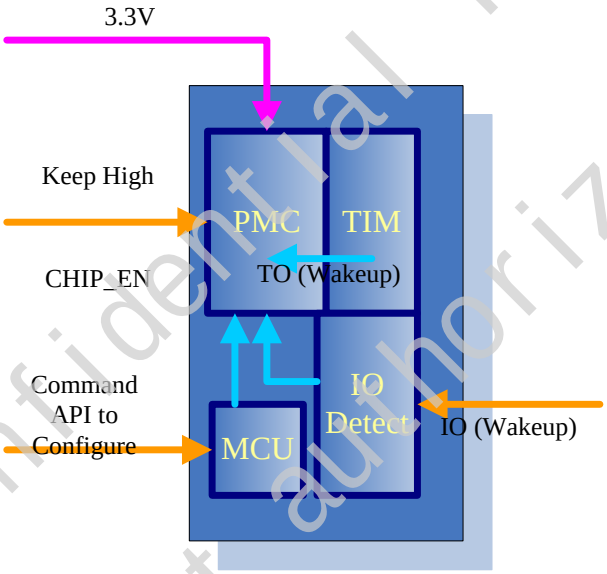
8.1.2.1 Shutdown Mode

CHIP_EN deasserts to shutdown whole chip without external power cut components required.



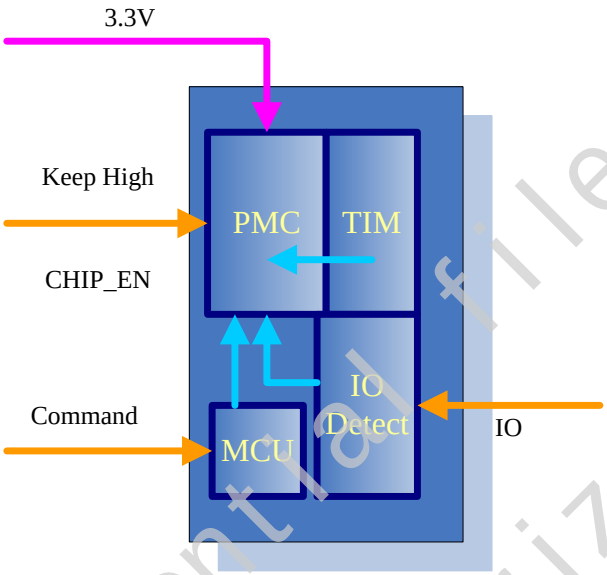
8.1.2.2 Deep Sleep Mode

CHIP_EN keeps high. Enter into Deep Sleep mode by API. The trigger timer period can be configured or GPIOB_1 can be used as external trigger event. The DLSP trigger timer can be configured with the range 1 ~ 3600 sec.



8.1.2.3 Deep Standby Mode

CHIP_EN keeps high. Entering into Deep Sleep mode by API. The trigger timer period can be configured or all GPIO group can be used as external trigger event.



8.2. Memory System

8.2.1. Memory Architecture

RTL8711AF integrates ROM, internal SRAM, extended NOR flash to provide applications with a variety of memory requirements.

8.2.2. Internal ROM

RTL8711AF integrates 1MB ROM to provide high access speed, low leakage memory. The ROM memory clock speed is up to 166MHz. The ROM lib provides the following functions:

- Boot Code and MCU initialization
- Default UART driver
- Non-flash booting functions and drivers
- Peripheral libs
- Security function libs

8.2.3. Internal SRAM

448KB SRAM is integrated to provide instruction, data, and buffer usage. The maximum clock speed is up to 166MHz.

Additional 64KB fast access data memory (TCM) is provided for FW data section. The range is 0x1FFF-0000 ~ 0x1FFF-FFFF.

8.2.4. SPI NOR Flash

Features

- Targeted SPI flash frequency: Up to 83.3MHz (when CPU clock is 166MHz)
- In addition to a programmed I/O interface, also supports a memory-mapped I/O interface for read operation
- Supports Read and Fast Read in memory-mapped I/O mode

Electrical Specifications

Table 10. Flash Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	1
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	2
V_{OH}	Output-High Voltage	-	2.4	-	-	V	3
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	3
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	μA	-
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	μA	-
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	4
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	4

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes

Note 1: V_{IH} overshoot: VIH (MAX)=VDDH + 2V for a pulse width ≤3ns.

Note 2: V_{IL} undershoot: $V_{IL\ (MIN)=}$-2V for a pulse width ≤3ns.

Note 3: The output current buffer is 8mA for the flash address and data bus; and is 8mA for Flash control signals.

Note 4: These values are typical values checked in the manufacturing process and are not tested.

8.3. General Purpose DMA Controller

8.3.1. Features of GDMA

- Dual port DMA with totally 12 channels
- Configurable endian
- Support memory-memory, memory-peripheral, peripheral-memory, and peripheral-peripheral DMA transfer
- Support block level flow control
- Support address auto-reload, link-listed mode
- Support scatter-gather mode

8.4. General Purpose Timer

8.4.1. Features of GTimer

- 8 Gtimer supported
- Source clock is 32.768KHz
- Support Counter mode and timer mode

8.5. GPIO Functions

8.5.1. Features of GPIO

- GPO and GPI function
- Support interrupt detection with configurable polarity per GPIO
- Internal weak pull up and pull low per GPIO
- Multiplexed with other specific digital functions

8.6. UART Interface Characteristics

The RTL8711AF UART is used for serial communication with a peripheral, modem (data carrier equipment, or data set.

8.6.1. Features of UART

- Support maximum 2 HS-UART (max baud rate 4MHz and DMA mode) and 1 low speed UART (IO mode)
- UART (RS232 Standard) Serial Data Format
- Transmit and Receive Data FIFO
- Programmable Asynchronous Clock Support
- Auto Flow Control (HS-UART only)
- Programmable Receive Data FIFO Trigger Level (HS-UART only)
- DMA data moving support to save CPU loading (HS-UART only)

8.6.2. High Speed UART Specification

The HS-UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. The default baud rate is

115.2k baud. In order to support high and low speed baud rate, the RTL8711AF provides multiple UART clocks.

Table 11. UART Baud Rate Specifications

Desired Baud Rate	Actual Baud Rate	Error (%)
300	300	0.00%
600	600	0.00%
900	900	0.00%
1200	1200	0.00%
1800	1800	0.00%
2400	2400	0.00%
3600	3601	0.03%
4800	4798	-0.04%
7200	7198	-0.03%
9600	9603	0.03%
14400	14395	-0.03%
19200	19182	-0.09%
28800	28846	0.16%
38400	38462	0.16%
56000	55970	-0.05%
57600	57692	0.16%
76800	76531	-0.35%
115200	115385	0.16%
128000	127119	-0.69%
153600	153061	-0.35%
230400	229167	-0.54%
460800	458333	-0.54%

Desired Baud Rate	Actual Baud Rate	Error (%)
500000	500000	0.00%
921600	916667	-0.54%
1000000	1000000	0.00%
1382400	1375000	-0.54%
1444444	1437500	-0.48%
1500000	1500000	0.00%
1843200	1833333	-0.54%
2000000	2000000	0.00%
2100000	2083333	-0.79%
2764800	2777778	0.47%
3000000	3000000	0.00%
3250000	3250000	0.00%
3692300	3703704	0.31%
3750000	3750000	0.00%
4000000	4000000	0.00%

8.6.3. Low Speed UART Specification

Data is written from CPU over the bus to the LS-UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the LS-UART and stored for the CPU to read back. The LS-UART can not support HW flow control.

Table 12. LS-UART Baud Rate Specifications

Desired Baud Rate	Actual Baud Rate	Error (%)
600	600	0.01
1200	1200	0.01
2400	2400	0.01
4800	4796	0.09
9600	9609	0.10
14400	14388	0.09
19200	19148	0.27
38400	38297	0.27
57600	57870	0.47
115200	115741	0.47

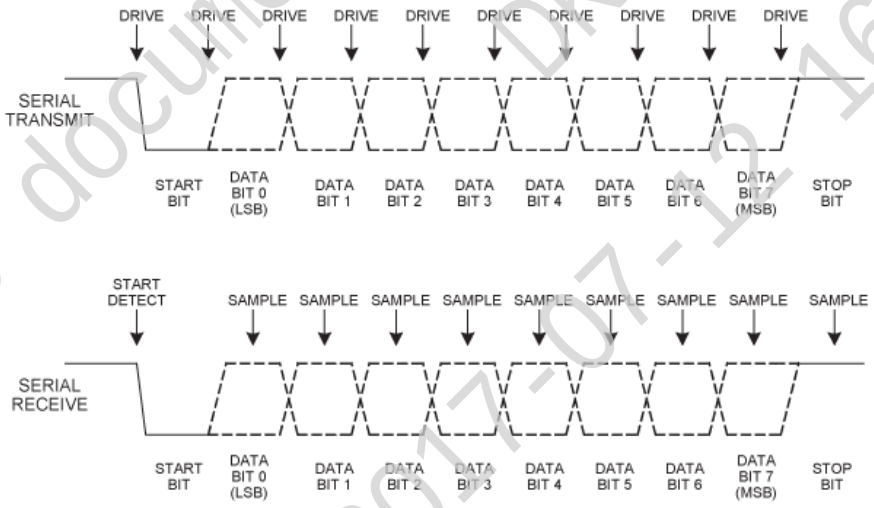


Figure 5. UART Interface Waveform

8.6.4. UART Interface Signal Levels

The UART signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8711AF UART interface via the IO power.

8.7. SPI Interface

8.7.1. Features of SPI

- Support maximum 2 SPI port
- Support Master/Slave mode (SPI0 only), and Master only (SPI1)
- Support DMA to offload CPU bandwidth
- 1 very high speed SPI (Master only)
  - Support up to 3 CS (multi-slave mode up to 3 slave)
  - Support baud rate up to 41MHz (Master mode)
- 1 high speed SPI (Master/Slave)
  - Support baud rate up to 20MHz (Master mode)
  - Support baud rate up to 5MHz (Slave mode Rx only)
  - Support baud rate up to 4MHz (Slave mode TRx)
- Programmable clock bit-rate
- Programmable clock polarity and phase
- Multiple Serial Interface Operations support
  - Motorola - SPI
  - Texas Instruments - SSI
  - National Semiconductor - Microwire

8.8. I2C Interface

8.8.1. Features of I2C

- Support maximum 3 I2C port
- Three speeds:
  - Standard mode (0 to 100 Kb/s)
  - Fast mode (<400 Kb/s)
  - High-speed mode (<3.4 Mb/s) (with appropriate bus loading)
- Master or Slave I2C operation
- 7- or 10-bit addressing
- Transmit and receive buffers
- TX and RX DMA support (I2C 0 and 1 only)

8.9. PWM Interface

8.9.1. Features of PWM

- Support maximum 4 PWM functions
- 0~100% duty can be configurable
- Minimum resolution is 64us
- The period can be configured up to 8 seconds

8.10. External Trigger Event Interface

8.10.1. Features of External Trigger Event

- Support maximum 4 External Trigger Event functions without CPU active

- Triggered by GTIMER

8.11. SDIO/RTK SPI Device Mode Interface

8.11.1. Features of SDIO/RTK SPI Device Mode Interface

- Support SDIO 2.0 SDR25
- CIS can be configured with internal non-volatile memory for fast card detection
- RTK SPI provides high efficiency SPI interface with interrupt and full duplex mode
- Support high performance Ethernet to WIFI transformation
- Support non-flash booting in the use of Ethernet to WIFI transformation card

8.11.2. SDIO Device Mode Specifications

8.11.2.1 Bus Timing Specification

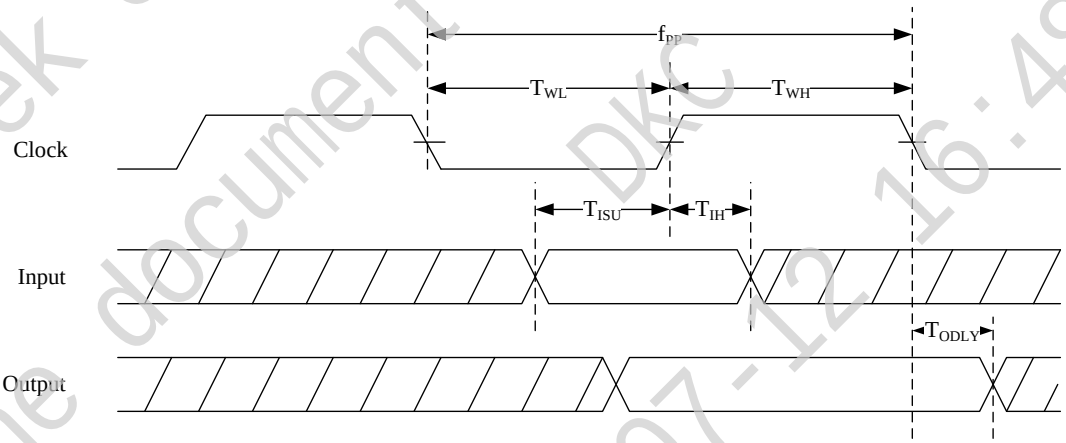


Figure 6. SDIO Interface Timing

Table 13. SDIO Interface Timing Parameters

NO	Parameter	Mode	MIN	MAX	Unit
f_{PP}	Clock Frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock Low Time	DEF	10	-	ns
		HS	7	-	ns
T_{WH}	Clock High Time	DEF	10	-	ns
		HS	7	-	ns
T_{ISU}	Input Setup Time	DEF	5	-	ns
		HS	6	-	ns
T_{IH}	Input Hold Time	DEF	5	-	ns
		HS	2	-	ns
T_{ODLY}	Output Delay Time	DEF	-	14	ns
		HS	-	14	ns

8.12. I2S Interface

8.12.1. Features of I2S

- Support 8/16/24/32/48/96KHz, 44.1/88.2KHz
- Support 16 or 24 bits format
- Integrated DMA engine to minimize SW efforts
- Support TX and RX direction
- Master or Slave mode support

8.13. PCM Interface

8.13.1.1 Features of PCM

The RTL8711AF supports 2 PCM digital audio interface that are used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit A-law/μ-law, and 13/16-bit linear PCM formats
- Supports sign-extension and zero-padding for 8-bit and 13-bit samples
- Supports padding of Audio Gain to 13-bit samples
- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports SCO/ESCO link

8.13.2. PCM Specifications

8.13.2.1 PCM Format

FrameSync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data. A Long FrameSync indicates the start of ADC_Data at the rising edge of FrameSync, and a Short FrameSync indicates the start of ADC_Data at the falling edge of FrameSync

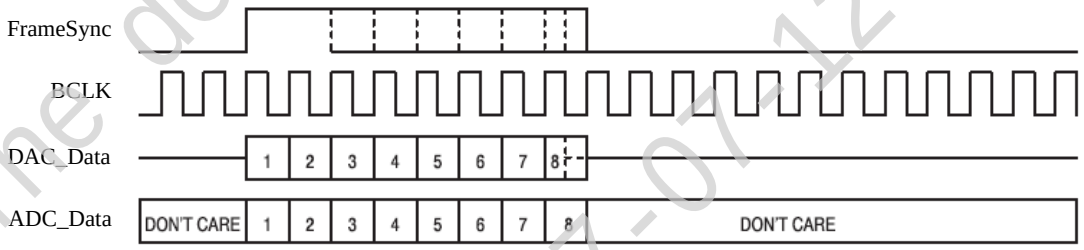


Figure 7. Long FrameSync

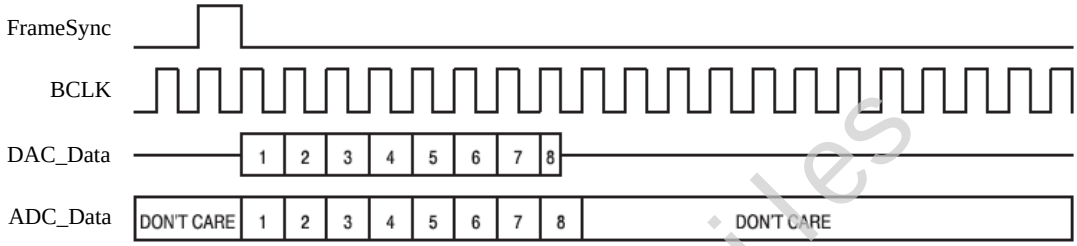


Figure 8. Short FrameSync

8.13.2.2 Sign Extension and Zero Padding for 8-Bit and 13-Bit Samples

For 16-bit linear PCM output, 3 or 8 unused bits may be sign extended/zero padded.

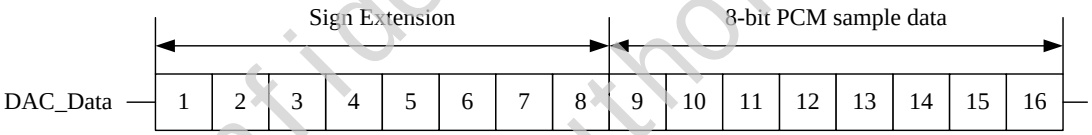


Figure 9. 16-Bit Output Data with 8-Bit PCM Sample Data and Sign Extension

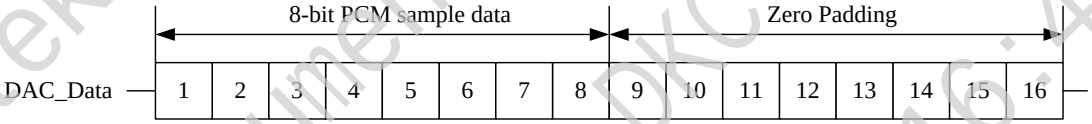


Figure 10. 16-Bit Output Data with 8-Bit PCM Sample Data and Zero Padding

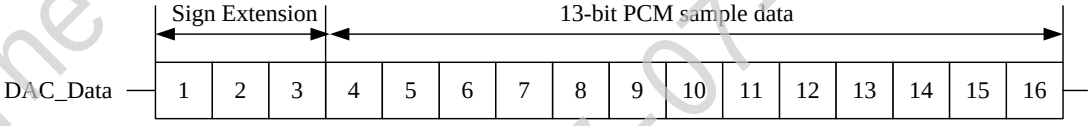


Figure 11. 16-Bit Output Data with 13-Bit PCM Sample Data and Sign Extension

For 16-bit linear PCM output, 3-bit programmable audio gain value can be padded to 13-bit sample data.

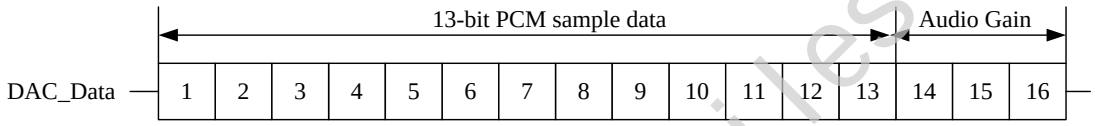


Figure 12. 16-Bit Output Data with 13-Bit PCM Sample Data and Audio Gain

8.13.2.3 PCM Interface Timing

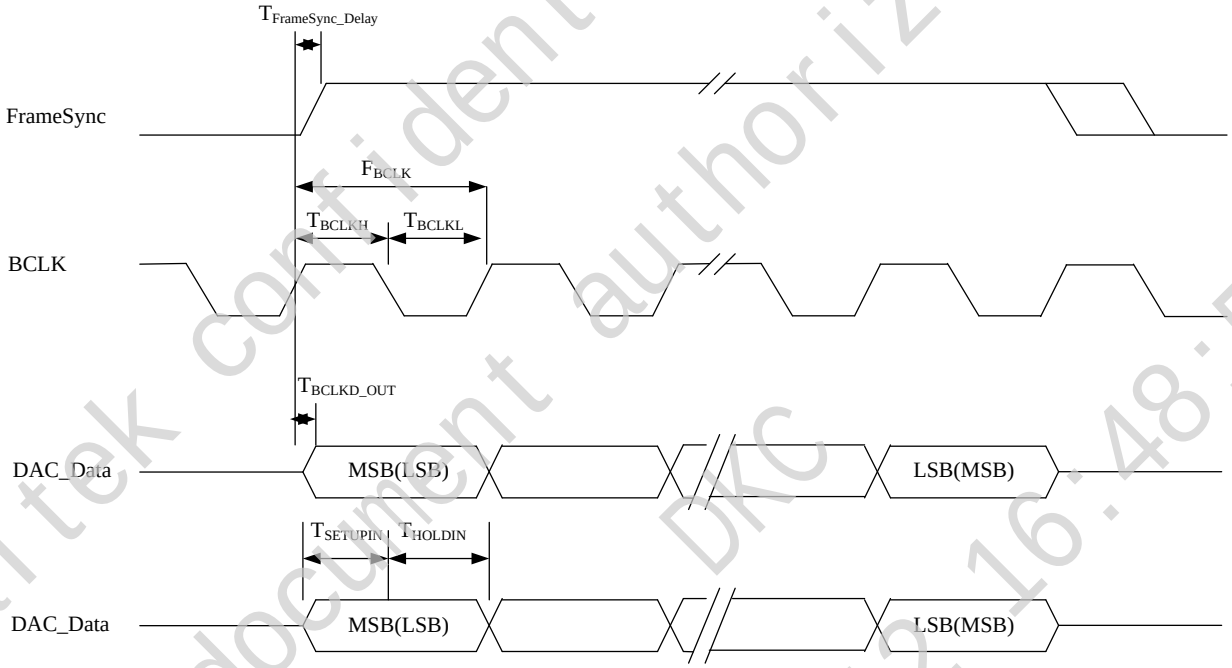


Figure 13. PCM Interface (Long FrameSync)

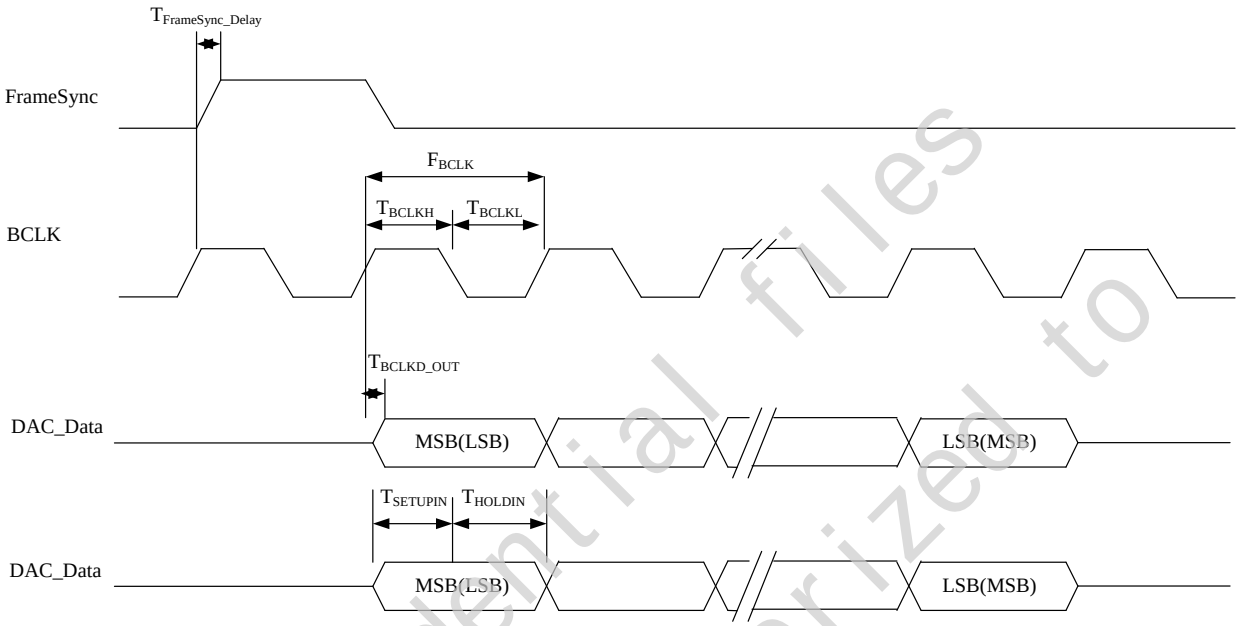


Figure 14. PCM Interface (Short FrameSync)

Table 14. PCM Interface Clock Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
F_{BCLK}	Frequency of BCLK (Master)	64	-	512	kHz
$F_{FrameSync}$	Frequency of Frame Sync (Master)	-	8	-	kHz
F_{BCLK}	Frequency of BCLK (Slave)	64	-	512	kHz
$F_{FrameSync}$	Frequency of Frame Sync (Slave)	-	8	-	kHz
D	Data Size	8	8	16	bits
N	Number of Slots Per Frame	1	1	1	Slots

Table 15. PCM Interface Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{BCLKH}	High Period of BCLK	980	-	-	ns
T_{BCLKL}	Low Period of BCLK	970	-	-	ns

Symbol	Description	Min.	Typ.	Max.	Unit
$T_{FrameSync\_Delay}$	Delay Time from BCLK High to Frame Sync High	-	-	75	ns
T_{BCLKD_OUT}	Delay Time from BCLK High to Valid DAC_Data	-	-	125	ns
$T_{SETUPIN}$	Set-up Time for ADC_Data Valid to BCLK Low	10	-	-	ns
T_{HOLDIN}	Hold Time for BCLK Low to ADC_Data Invalid	125	-	-	ns

8.13.2.4 PCM Interface Signal Levels

The PCM signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8711AF PCM interface via the VDD_IO pin.

8.14. Security Engine

8.14.1. Features

- Provide low SW computing and high performance encryption
- Supported authentication algorithms:
  - MD5
  - SHA-1
  - SHA-2 (SHA-224 / SHA-256)
  - HMAC-MD5
  - HMAC-SHA1
  - HMAC-SHA2

-
- Supported Encryption / Decryption mechanisms:
  - DES (CBC / ECB)
  - 3DES (CBC / ECB)
  - AES-128 (CBC / ECB / CTR)
  - AES-192 (CBC / ECB / CTR)
  - AES-256 (CBC / ECB / CTR)

9. Electrical Characteristics

9.1. Temperature Limit Ratings

Table 16. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	-20	+85	°C
Junction Temperature	0	+125	°C

9.2. Temperature Characteristics

Table 17. Thermal Properties

Power (w)	PCB (layer)	Theta ja (C/W)	Theta jc (C/W)	Psi jt (C/W)
1	2	38.7	12.4	0.35
1	4	28.1	11.1	0.24

9.3. Power Supply DC Characteristics

Table 18. Power Supply DC Characteristics

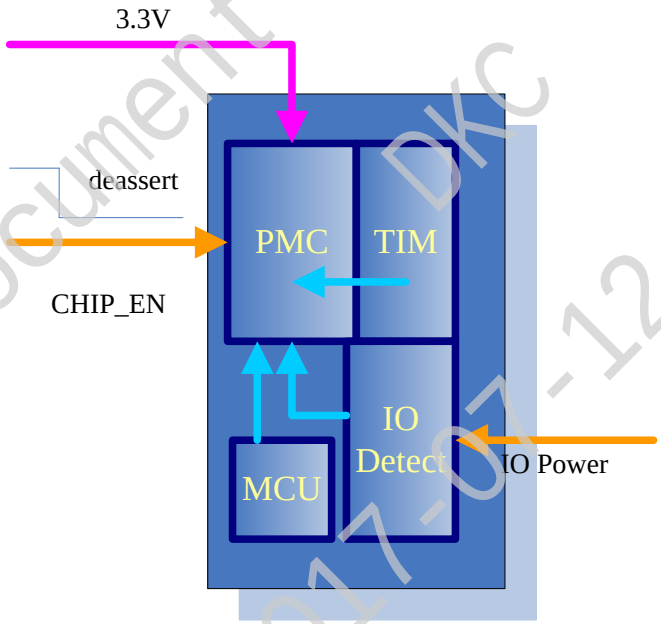
Symbol	Parameter	Minimum	Typical	Maximum	Units
VA33, VD33IO, SW_HV3	3.3V Supply Voltage	3.0	3.3	3.6	V
VDD_IO	Digital IO Supply Voltage	1.62	1.8~3.3	3.6	V

Symbol	Parameter	Minimum	Typical	Maximum	Units
VA12_AFE, VA12_SYN, VA12_RF	1.2V Core Supply Voltage	1.08	1.2	1.32	V
IDD33	3.3V Rating Current (with internal regulator and integrated CMOS PA)	-	-	450	mA
IDD_IO	IO Rating Current (including VDD_IO)			200	mA
IDD_IO_33	3.3V IO Rating Current			50	mA

9.3.1. Power Mode Description

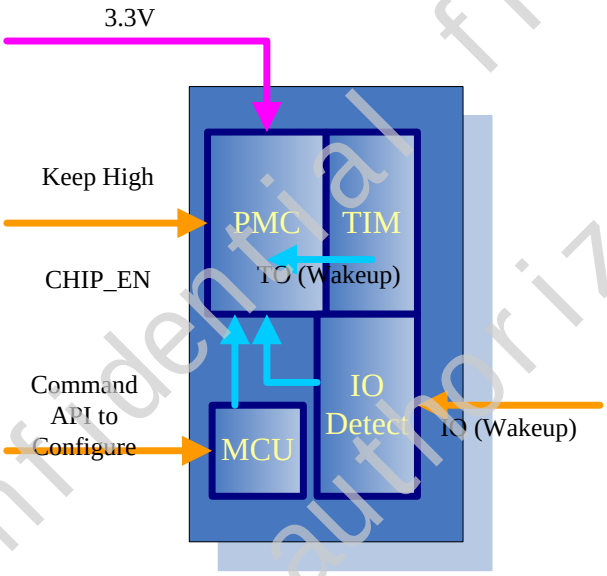
- Shutdown Mode

CHIP_EN deasserts to shutdown whole chip without external power cut components required.



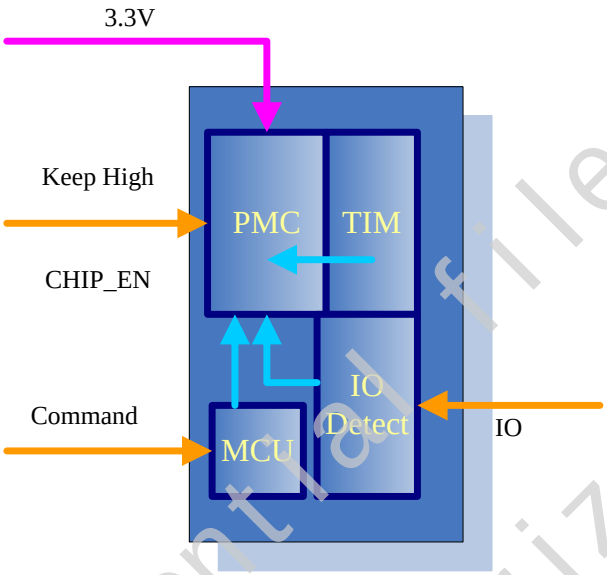
■ Deep Sleep Mode

CHIP_EN keeps high. Enter into Deep Sleep mode by API. The trigger timer period can be configured or GPIOB_0 can be used as external trigger event. The DLSP trigger timer can be configured with the range 1 ~ 3600 sec.



■ Deep Standby Mode

CHIP_EN keeps high. Entering into Deep Sleep mode by API. The trigger timer period can be configured or all GPIO group can be used as external trigger event.



9.4. Power Sequence

9.4.1. Power On or Resume from Deep Sleep

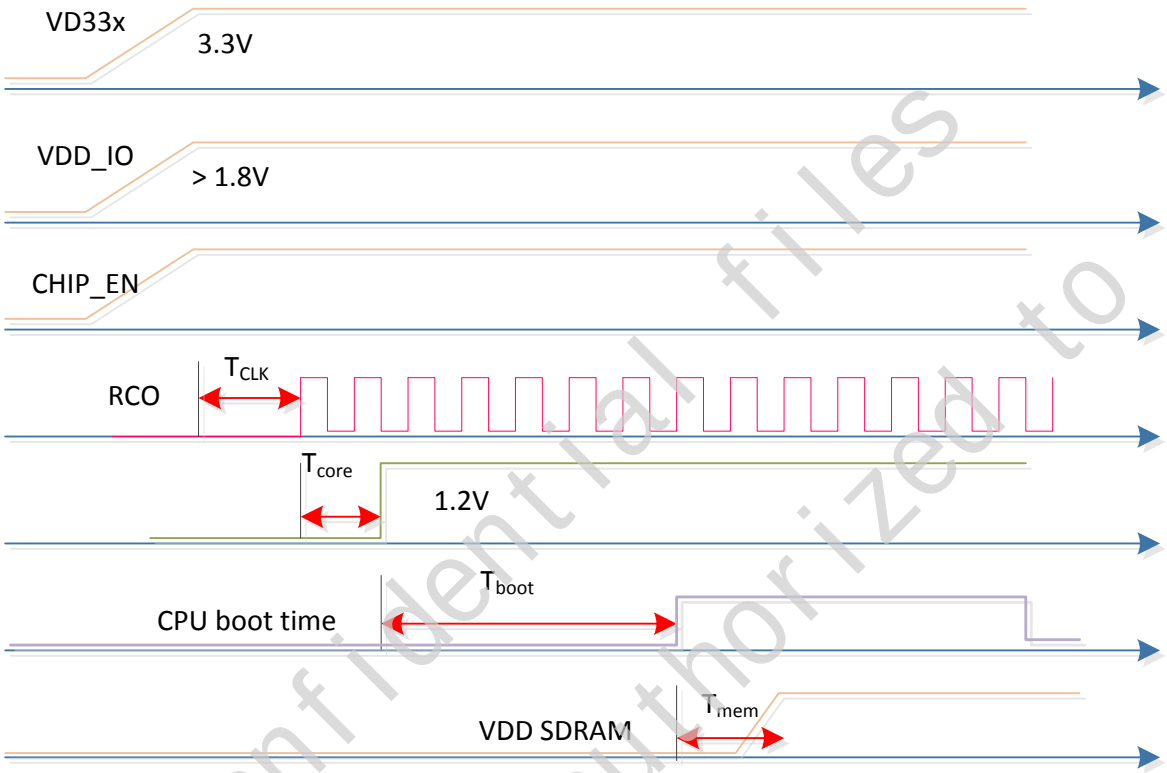


Figure 15. Power-On Sequence or Resume from Deep Sleep

Table 19. Timing spec for power on sequence

Symbol	Parameter	Minimum	Typical	Maximum	Units
T_{CLK}	Internal ring clock stable time after 3.3V ready	1			ms
T_{core}	Core power ready time	1.5	1.5		ms
T_{boot}	1.2V Core Supply Voltage	200	200		ms

T_{mem}: SW controlled memory power ready time.

9.4.2. Resume from Deep Standby

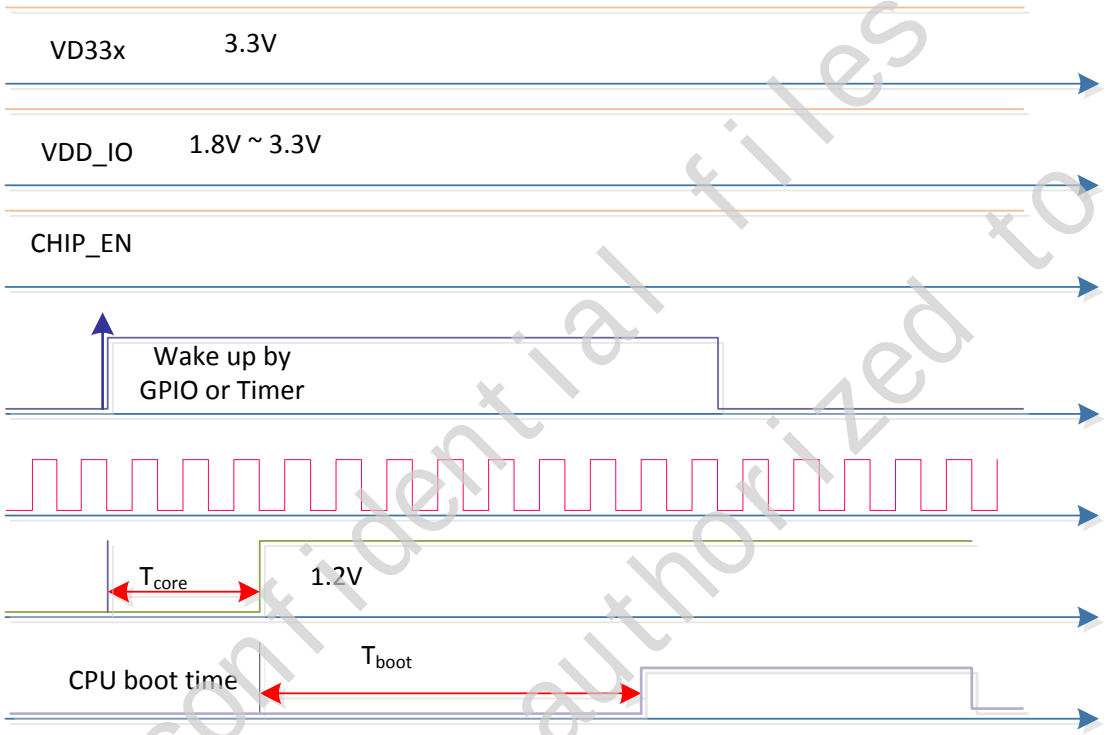


Figure 16. Timing Sequence resume from Deep Standby

9.5. Digital IO Pin DC Characteristics

9.5.1. Electrical Specifications

Table 20. Typical Digital IO DC Parameters (3.3V Case)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V
V_{OH}	Output-High Voltage	LVTTL	2.4	-	-	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OL}	Output-Low Voltage	LVTTL	-	-	0.4	V
V_{T+}	Schmitt-trigger High Level		1.78	1.87	1.97	V
V_{T-}	Schmitt-trigger Low Level		1.36	1.45	1.56	V
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	μA

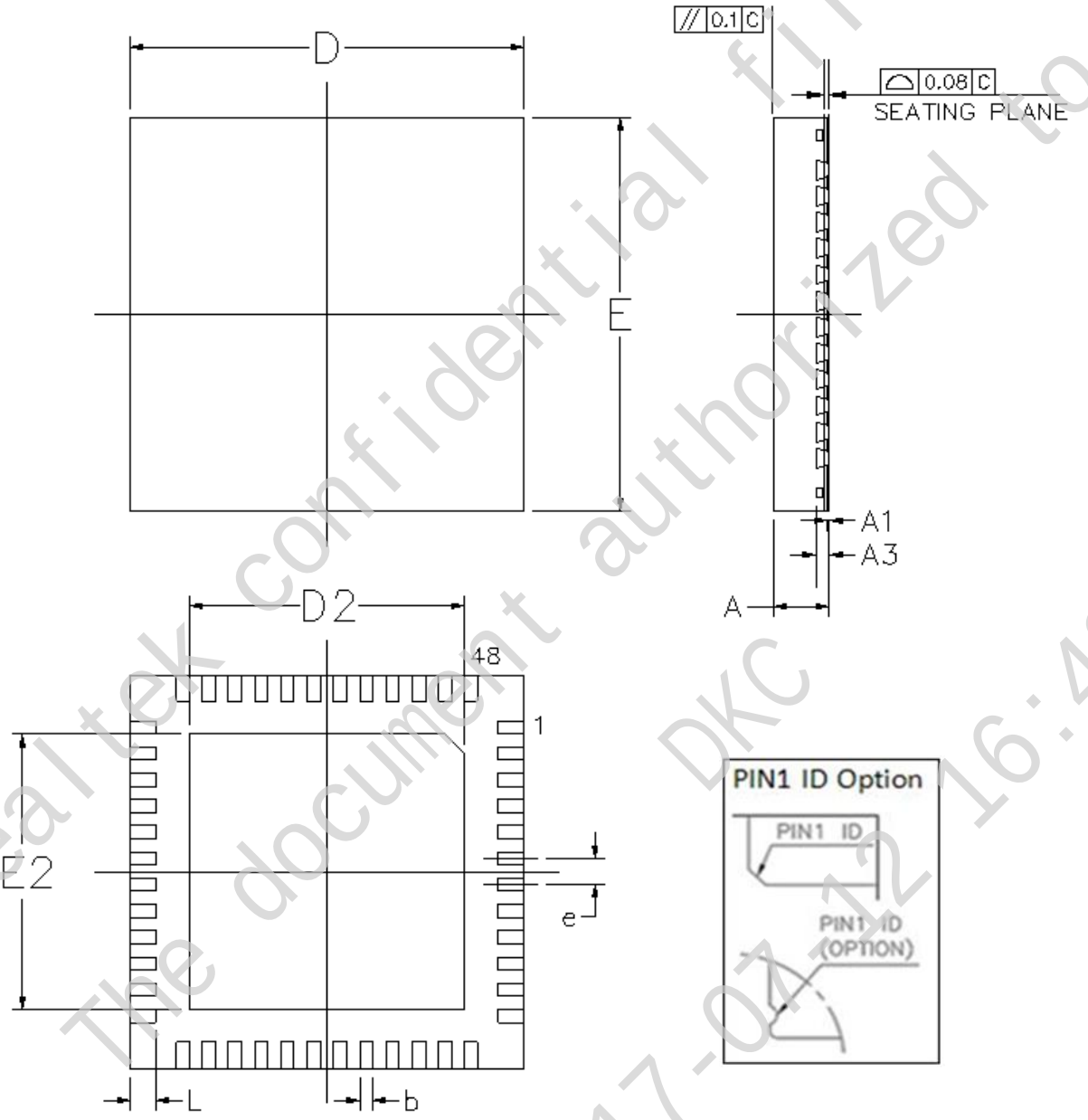
-

Table 21. Typical Digital IO DC Parameters (1.8V Case)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	CMOS	0.65x V_{CC}	-	-	V
V_{IL}	Input-Low Voltage	CMOS	-	-	0.35x V_{CC}	V
V_{OH}	Output-High Voltage	CMOS	V_{CC}-0.45	-	-	V
V_{OL}	Output-Low Voltage	CMOS	-	-	0.45	V
V_{T+}	Schmitt-trigger High Level		1.02	1.09	1.14	V
V_{T-}	Schmitt-trigger Low Level		0.67	0.73	0.8	V
I_{IL}	Input-Leakage Current	V_{IN}=1.8V or 0	-10	±1	10	μA

9.6. Mechanical Dimensions

9.6.1. Package Specification



9.6.2. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	6.00BSC			0.236BSC		
D2/E2	4.15	4.4	4.65	0.163	0.173	0.183
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

9.7. Digital IO Pin DC Characteristics

9.7.1. Electrical Specifications

Table 22. Typical Digital IO DC Parameters (3.3V Case)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V
V_{OH}	Output-High Voltage	LVTTL	2.4	-	-	V
V_{OL}	Output-Low Voltage	LVTTL	-	-	0.4	V
V_{T+}	Schmitt-trigger High Level		1.78	1.87	1.97	V
V_{T-}	Schmitt-trigger Low Level		1.36	1.45	1.56	V
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	μA

Table 23. Typical Digital IO DC Parameters (1.8V Case)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	CMOS	0.65x V_{CC}	-	-	V
V_{IL}	Input-Low Voltage	CMOS	-	-	0.35x V_{CC}	V
V_{OH}	Output-High Voltage	CMOS	V_{CC}-0.45	-	-	V
V_{OL}	Output-Low Voltage	CMOS	-	-	0.45	V
V_{T+}	Schmitt-trigger High Level		1.02	1.09	1.14	V
V_{T-}	Schmitt-trigger Low Level		0.67	0.73	0.8	V
I_{IL}	Input-Leakage Current	V_{IN}=1.8V or 0	-10	±1	10	µA

10. Ordering Information

Table 24. Ordering Information

Part Number	Package	Status
RTL8711AF-VB1-CG	QFN48	MP